EXPRESS MAIL LABEL NO:
EM 004 869 724 US

PROCESS FOR DEPOSITING F-DOPED SILICA GLASS IN HIGH ASPECT RATIO STRUCTURES

George D. Papasouliotis
Robert D. Tas
Patrick A. Van Cleemput
Bart van Schravendijk

CROSS REFERENCE TO RELATED APPLICATIONS

This application is a continuation-in-part application of U.S. Pat. Appl. Serial No. 09/053,554, filed April 1, 1998.

FIELD OF THE INVENTION

The present invention relates generally to methods of thin film deposition and, particularly, to a process of filling high aspect ratio gaps on substrates using high density plasma (HDP) chemical vapor deposition (CVD).

DESCRIPTION OF RELATED ART

Integrated circuits fabricated on semiconductor substrates for large scale integration require multiple levels of metal interconnections to electrically interconnect the discrete layers of semiconductor devices on the semiconductor chips. The different levels of interconnections are separated by various insulating or dielectric layers, which have etched via holes to connect one level of metal to the next. Typically, the insulating layer is a silicon oxide having a dielectric constant k of approximately 4.1 to approximately 4.5.

However, as semiconductor technology advances, circuit elements and dimensions on wafers or silicon substrates are becoming increasingly more dense. Consequently, the spacing between the metal lines in the interconnections needs to be reduced to effectively connect the various circuit elements. By decreasing the thickness of the insulating layers, intralevel and interlevel capacitances between the metal lines increase, since the capacitance is inversely proportional to the spacing between the lines. As capacitance increases, the RC time delay increases, which decreases the frequency response of the circuit and increases the signal propagation time through the circuit, thereby adversely affecting circuit performance. Therefore, it is desirable to minimize the RC time constant. One approach to reduce these RC time delays is to use an insulating material having a lower dielectric constant k to reduce the capacitance between the metal lines. Low-k layers also help to prevent cross-talk between different metal layers and reduce device power consumption.

One method to reduce the dielectric constant is to incorporate fluorine or other halogen elements such as chlorine or bromine into the silicon oxide layer. Fluorine-doped silicon oxide layers or films are commonly referred to as fluorosilicate glass (FSG) films. Using FSG films can typically reduce the dielectric constant down to about 3.5.

In addition to decreasing the dielectric constant, incorporating fluorine in silicon oxide layers also helps solve common problems encountered in fabricating smaller geometry devices with increasingly more dense

circuit elements. In order to prevent unwanted interactions between these circuit elements, insulator-filled gaps or trenches located therebetween are provided to physically and electrically isolate the elements and conductive lines. However, as circuit densities continue to increase, the widths of these gaps decrease further, thereby increasing gap aspect ratios, typically defined as the gap height divided by the gap width. As a result, filling these narrower gaps becomes more difficult, which can lead to unwanted voids and discontinuities in the insulating or gap-fill material.

Currently, high density plasma (HDP) oxide deposition is used to fill high aspect ratio gaps. Generally, a high density plasma is any plasma having electron density greater or equal to $5x10^9$ electrons per cubic centimeter. Typical HDP deposition processes employ chemical vapor deposition (CVD) with a gas mixture containing oxygen, silane, and argon to achieve simultaneous dielectric etching and deposition. In an HDP process, an RF bias is applied to a wafer substrate in a reaction chamber. Some of the gas molecules (particularly argon) in this gas mixture are ionized in the plasma and accelerate toward the wafer surface when the RF bias is applied to the substrate. Material is thereby sputtered when the ions strike the surface. As a result, dielectric material deposited on the wafer surface is simultaneously sputter-etched to help keep gaps open during the deposition process, which allows higher gap aspect ratios to be filled.

Figs. 1A-1D illustrate, in more detail, the simultaneous etch and deposition (etch/dep) process

described above. In Fig. 1A, SiO_2, formed from silane (SiH_4) and oxygen (O_2), begins depositing on the surface of a wafer 100 for filling a gap 110 between circuit elements 120. As the SiO_2 is being deposited, charged ions impinge on the SiO_2 or dielectric layer 125, thereby simultaneously etching the SiO_2 layer. However, because the etch rate at about 45° is approximately three to four times the etch rate on the horizontal surface, 45° facets 130 form at the corners of elements 120 during the deposition process, as shown in Fig. 1B. Figs. 1C and 1D show the process continuing to fill gap 110 with simultaneous etching and deposition of SiO_2.

In Figs. 1A-1D, the etch/dep ratio is optimized such that facets 130 remain at the corners of circuit elements 120 throughout the HDP deposition process. However, as shown in Fig. 2A, if the etch/dep ratio is decreased, facets 130 begin moving away from the corners of elements 120, and cusps 210 begin to form on sidewalls of gap 110. Cusp formation is due to some of the etched SiO_2 being redeposited on opposing surfaces through line-of-sight redeposition, even though most of the etched SiO_2 is emitted back into the plasma and pumped out of the reaction chamber. This redeposition increases as the distance between opposing surfaces decreases. Therefore, as facets 130 move away from the corners of elements 120, the line-of-sight paths are shortened, resulting in increased sidewall redeposition. At a certain point in the process, cusps 210 will meet and prevent further deposition below the cusps. When this occurs, a void 220 is created in dielectric layer 125, as shown in Fig. 2B. On the other hand, if the etch/dep ratio is increased, as

shown in Fig. 3, the etching component can etch or "clip" material from the corners of elements 120, thereby damaging elements 120 and introducing etched contaminants 310 into dielectric layer 125.

The etch/dep ratio can be controlled by varying the flow rate of silane or other process gases, which affect the deposition rate, or by varying either the power supplied to the wafer for biasing or the flow rate of argon, which affect the sputter etch rate. Etch rates are typically increased by increasing the flow rate of argon, which is used solely to promote sputtering, rather than increasing power and expending large amounts of energy. Typical argon flow rates for HDP deposition range from 30%-60% or more of the total process gas flow rate. By optimizing the etch/dep ratio, gaps with aspect ratios of up to about 3.0:1 can be filled without void formation. However, as shown in Fig. 4, filling higher gap aspect ratios results in voids 410 due to cusps 420 prematurely closing the gaps even if the etch/dep ratio is optimized to 1 at the element corners. As discussed above, this is due mainly to the shortened line-of-sight path between opposing sidewalls. If the etch rate is increased to keep the gaps open longer, undesirable corner clipping can occur.

Therefore, with increasing circuit densities, higher gap aspect ratios need to be filled using fluorine-doped films without the problems discussed above with current HDP deposition processes.

SUMMARY

In accordance with the present invention, a high aspect ratio gap-fill process uses high density plasma (HDP) deposition processes with helium, hydrogen, or other inefficient sputtering gases, instead of argon to reduce the effects of sputtering and redeposition for depositing fluorine-doped films, such as FSG (F-doped silica glass). Because the sputtering agent is greatly reduced, the etch or sputter rate decreases and the facet moves away from the element corners, as expected. Cusps form to a lesser extent on the element sidewalls because much less material is etched and available for redeposition. Consequently, with a greatly reduced sputter component, gaps remain open longer so that higher aspect ratio gaps can be filled without the formation of voids. The gas mixture can include both hydrogen and helium in some embodiments.

Because oxygen also contributes to the sputtering component, reducing the partial pressure of oxygen further reduces the sputtering and redeposition effect and allows increased gap-fill capabilities. However, in order to preserve the stoichiometry of the film, the partial pressure of silane (SiH_4) is decreased as well. Helium, which is an inefficient sputtering agent, can be added to maintain a constant overall process gas flow rate and provide a constant uniform deposition rate across the wafer.

The present invention will be better understood in light of the following detailed description, taken together with the accompanying drawings.

BRIEF DESCRIPTION OF THE DRAWINGS

Figs. 1A-1D are sequential views of a conventional HDP deposition process with optimized etch/dep ratios;

Figs. 2A-2B are sequential views illustrating void formation when the etch/dep ratio decreases using a conventional HDP process;

Fig. 3 is a picture of "clipped" corners when the etch/dep ratio increases using conventional HDP processes;

Fig. 4 is a picture of void formation when filling a high aspect ratio gap using a conventional HDP process; and

Figs. 5A-5D are sequential views of high aspect ratio gaps filled with the method of the present invention.

Use of the same reference numbers in different figures indicates similar or like elements.

DETAILED DESCRIPTION

In accordance with an embodiment of the present invention, a process using high density plasma (HDP) deposition with helium, hydrogen, or other inefficient inert sputtering gases, is provided, which allows high aspect ratio gaps to be filled using fluorine-doped films without voids or clipped corners associated with conventional methods. In other embodiments, the gas mixture includes both helium and hydrogen.

Similar to conventional HDP deposition processes, a gas mixture is used containing silane (SiH_4), a fluorine-bearing precursor, and oxygen (O_2). However, contrary to conventional HDP processes, argon (Ar) is not used; rather an inefficient sputtering gas with an

atomic weight lower than Ar is used, such as helium (He), hydrogen (H_2), and/or neon (Ne). A mixture that includes SiH_4, O_2, a fluorine-bearing precursor, and hydrogen and/or He is used to simultaneously deposit and etch dielectric material, where SiH_4, O_2, and the fluorine-bearing precursor are used to form SiO_2 for the deposition component, and O_2 and He and/or hydrogen are used for the sputtering component. These gases are not limiting, and other suitable gases include any gases normally used for a particular film deposition process. As will be described below, adding SiF_4 or another fluorine-containing compound, such as Si_2F_6, to the gas mixture results in a fluorine-doped film, which as an advantage of a low dielectric constant. As will be described below, fluorine-doped films of low dielectric constant can be deposited by adding SiF_4 or another fluorine-containing compound, such as Si_2F_6 or SiH_2F_2, to the gas mixture.

By replacing Ar with He and/or hydrogen, the sputtering and redeposition effect is greatly reduced. Further, since O_2 also contributes to sputtering, reducing the partial pressure of O_2 further reduces sputtering. Accordingly, less material is sputtered and redeposited, thereby allowing even higher aspect gap ratios to be filled. However, by reducing the partial pressure of O_2, the partial pressure of SiH_4 must also be reduced proportionally if the stoichiometry of the film is to be preserved. As a result of the partial pressures of both O_2 and SiH_4 being reduced, the flow rate of the process gas decreases. Thus, in order to preserve the uniformity of the deposition rate across the wafer, He or another

low weight inert gas, is added to maintain a constant overall process flow rate.

As an example, the present invention is used to form a gap-free fluorine-doped silicon oxide (FSG) film over high aspect gap ratios. Incorporating fluorine reduces the dielectric constant of the deposited film. Table 1 below lists typical gases and their respective gas flow ranges for forming an FSG film in an HDP-CVD reactor, where the actual gas flow amount depends upon the requirements of the film and the wafer size. Hydrogen and/or He also acts as a diluent in the gas mixture.

Gas	Flow Rate (sccm)
SiH_4	10-250
O_2	10-1000
He	0-2000
SiF_4	10-250
Ne	0-2000
H_2	0-5000
N_2	0-500
Ar	0-100

Table 1

Those skilled in the art will recognize that Ar does not need to be completely eliminated if the concentration of He and/or hydrogen is high enough to dilute the effects of sputtering and redeposition in accordance with the present invention. Note that in

Table 1 above, both He and hydrogen have a lower range of 0 sccm. However, as those skilled in the art will understand, He and hydrogen are never both at 0 sccm. If only He is used, hydrogen will be at 0 sccm, and if only hydrogen is used, He will be at 0 sccm. When hydrogen is used, the low range of hydrogen flow is 5 sccm. In some embodiments, a conventional substrate holder having an electrode is used to support the wafer. A radio frequency (RF) bias is applied to the substrate by supplying the electrode with at least 0.15 W/cm^2 of power. The RF frequency ranges between about 100 kHz and 27 MHz.

In addition to the reduction or elimination of Ar, the method of the present invention also allows lower pressures than prior HDP processes. The present invention can be run at pressures below 10 mTorr. Other system parameters are similar to conventional FSG film deposition. For example, the LF power typically varies from 1 kW to 15 kW, and the HF power typically varies from 0.5 kW to 10 kW depending on the wafer size (e.g., 200 or 300 mm diameter) and the requirements of the specific process being used. The back-side He pressure is set by the temperature requirements of the process, with a typical range being between 0 and 15 Torr. Those skilled in the art will recognize that SiF_4 does not need to be the only fluorine-containing compound that can be used as a fluorine source. Other silicon fluorides (such as Si_2F_6 or SiH_2F_2) are within the scope of this invention. The inclusion of nitrogen in the reactive mixture is also within the scope of the invention.

The reduced sputter etch rate resulting from the replacement of Ar with He and/or hydrogen allows higher aspect ratio gaps to be filled without the formation of voids, as illustrated in Figs. 5A-5D.

In Fig. 5A, circuit elements 520 are formed on a substrate or wafer 100, creating gaps 510 therebetween. Circuit elements 520 can be, for example, transistors, conductors, or interconnects. A gap 510 with a high aspect ratio, typically greater than 2.5:1, is filled using HDP deposition, where sputtering is accomplished with He and/or hydrogen and O_2. During the initial stages of the process, 45° facets 530 form at the corners of circuit elements 520, as shown in Fig. 5A. Even though drastically reduced, an etching component from the He and/or hydrogen and O_2 still exists to form the facets 530 in Fig. 5A. However, because the etching component is reduced, facets 530 begin to move away from the corners of circuit elements 520 as more material deposits on the surfaces to form the FSG or dielectric layer 525, as shown in Figs. 5B and 5C.

Another consequence of replacing Ar with He and/or hydrogen is that sidewall redeposition is reduced. Because the sputtering component is greatly reduced, much less material is available to redeposit on sidewalls 540 and facets 530, as shown in Figs. 5B and 5C. As a result, cusp formation is drastically reduced, and facets move away more slowly from the corners of the circuit elements. Because there is very little sidewall deposition, which is mainly driven by redeposition, high aspect ratio gaps do not close prematurely even though the facets are moving away from the corners. Fig. 5D then shows high aspect ratio gap

510 filled without void formation or clipping. Note that since O_2 also acts as a sputtering agent, He and/or hydrogen can be used to reduce the sputtering effects from O_2.

In accordance with the present invention, gaps with aspect ratios greater than 3.0:1 and with spacing between lines less than 0.13 micron have been filled without the formation of voids. Therefore, by replacing an efficient sputtering agent such as Ar with an inefficient sputtering agent such as He and/or hydrogen, a void-free gapfill is possible at higher aspect ratios than are possible with conventional HDP deposition processes.

The above description illustrates the use of fluorine-doped silicon oxide for filling gaps between metal lines, such as in a BEOL (back-end-of-line) process in which electrical connections are made within the integrated circuit device. Using a fluorine-doped film results in many benefits, such as reduced signal delays, lower dielectric constants, and less cross-talk between layers. The method of the present invention can also be used in other steps in the production of integrated circuits where fluorine-doped films are deposited.

While particular embodiments of the present invention have been shown and described, it will be obvious to those skilled in the art that changes and modifications may be made without departing from this invention in its broader aspects. Therefore, the appended claims are to encompass within their scope all such changes and modifications as fall within the true spirit and scope of this invention.